

What is claimed is:

Sub A/

1. An integrated circuit characterized in that multi-
port data output signals are generated with respect to a data
input signal, and points of changing said data output signals
5 with respect to a time base are set with a time lag one another,
during one period of a reference internal clock signal, so that
number of simultaneous changes of display data output signals
is reduced.

Sub B/

10 2. An integrated circuit according to claim 1, wherein
the points of changing the data output signals with respect to
the time base are set to points respectively delayed from an
active edge of the clock output signal by 0.5 period, 1 period,
and 1.5 period of the data input signal.

Sub C/

15 3. An integrated circuit according to claim 1, wherein
the points of changing the data output signals with respect to
the time base are set to points respectively having a time lag
one another from the active edge of the clock output signal by
optional integer times as long as a half period of the data input
signal.

20 4. An integrated circuit according to claim 1, wherein
the points of changing the data output signals with respect to
the time base are set to points respectively having a time lag
one another from the active edge of the clock output signal by
optional integer times as long as a half period of the data input
25 signal and by a delay time produced by a delay circuit added

to the optional integer times as long as a half period of the data input signal.

5 5. A liquid crystal display characterized in that multi-port display data output signals are generated with respect to a data input signal, and points of changing said display data output signals with respect to a time base are set with a time lag one another during one period of a clock output signal or a reference internal clock signal having a same phase as the clock output signal, so that number of simultaneous changes of display data output signals is reduced.

10 6. A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively delayed from the active edge of the clock output signal by 0.5 period, 15 1 period, and 1.5 period of the clock input signal or the display data input signal.

20 7. A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively having a time lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the clock input signal or the display data input signal.

25 8. A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively having

a time lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the clock input signal or the display data input signal and by a delay time produced by a delay circuit added to the integer
5 times as long as the half period of the clock input signal or the display data input signal.

9. A driving method of a liquid crystal display characterized in that when red, green and blue color display data composed of plural bits are transferred from a display
10 timing circuit to a TFT drive circuit for driving a TFT liquid crystal panel to display, each transfer is performed with a time lag little by little for each bit unit formed of plural bits optionally selected from each of said color display data.

10. A driving method of a liquid crystal display according
15 to claim 9, wherein the bit unit is formed for each of red, green and blue color display data.

11. A driving method of a liquid crystal display according to claim 9, wherein each bit unit has a part of the plural bits forming the red, green and blue color display data.

20 12. A driving method of a liquid crystal display according to claim 9, wherein the bit unit is transferred with a time lag of 2 nanoseconds or longer.

13. A driver of a liquid crystal display comprising: a TFT drive circuit for driving a TFT liquid crystal panel to
25 display; a display timing control circuit for transferring red,

green and blue color display data formed of plural bits to the TFT drive circuit for each bit unit formed of plural bits optionally selected from each of the color display data; and a delay unit provided in the display timing control circuit to
5 delay the transfer timing between one bit unit and another.

14. A liquid crystal display comprising: a drive circuit for driving a display section; a data supply circuit for supplying image data through a signal line to said drive circuit; a detector circuit for detecting a coincidence of
10 polarity by comparing a polarity of bits for each predetermined group of image data outputted by the data supply circuit; a first control circuit for outputting the data of the group represented by certain data to said signal line when the coincidence of polarity has been detected by the detector circuit; and a second
15 control circuit for outputting the data of said group restored from the certain data of the signal line to the drive circuit when the coincidence of polarity of bit has been detected by the detector circuit.

15. A liquid crystal display according to claim 14,
20 wherein the predetermined group of image data are red, green and blue data.

16. A liquid crystal display according to claim 14, wherein the certain data are red data.

17. A liquid crystal display according to claim 14,
25 wherein the first control circuit controls the predetermined

group of data to be a low potential, except the certain data.

18. A liquid crystal display according to claim 14, wherein the second control circuit forms the predetermined group of data to be same as the certain data.

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ABSTRACT OF DISCLOSURE

1) There is provided an integrated circuit having a liquid crystal display of high quality capable of reducing electromagnetic wave noise in input/output signal sections and unnecessary electromagnetic wave negatively affecting other system or circuit, and having a multi-port data output section. Multi-port data output signals 9, 10, 11 are generated with respect to a data input signal 2, and points of changing the data output signals 9, 10, 11 with respect to a time base are set with a time lag one another during one period of a reference internal clock signal 3, whereby number of simultaneous changes of display data output signals is reduced.

2) In a TFT-LCD panel, when display data are transferred from a LCD timing controller to a source driver IC, electromagnetic field noise is reduced by a LCD driver. The driver comprises: a TFT drive circuit for driving a TFT liquid crystal panel to display; a display timing control circuit for transferring red, green and blue color display data formed of plural bits to the TFT drive circuit for each bit unit formed of plural bits optionally selected from each of the color display data; and a delay unit provided in the display timing

control circuit to delay the transfer timing between one bit unit and another.

3) In the conventional liquid crystal display, as data delivery between a dedicated IC and a source driver IC is performed by inversion of data taking place on condition that majority of the data are simultaneously changed, efficiency of data delivery is not always high. To solve this problem, there is provided a liquid crystal display comprising an dedicated IC for supplying image data through a signal line 15 to a source driver IC for driving a display section; a detector-comparator circuit 16 for detecting a coincidence of polarity by comparing a polarity for each bit of red, green and blue of the image data outputted by the dedicated IC; a control circuit A17 for outputting the red, green and blue data represented by red data to the signal line 15 when the coincidence of polarity has been detected by the detector-comparator circuit 16; and a control circuit B18 for outputting the green and blue data restored from the red data of the signal line 15 to the source driver IC when the coincidence of polarity of bit has been detected by the detector-comparator circuit 16.